Application Note 702: Mar 16, 2000

Choosing The Optimum Buffer/ADC Combination For Your Application

This article helps the designer of a data converter system to select the proper input buffer to achieve optimum performance. Numerous parameters and their effect on data converter performance are discussed including; noise, distortion, bandwidth, settling time, gain flatness, slew rate, SFDR, current drive, offset voltage, loop gain, and output impedance.

Selecting the optimum drive amplifier (or buffer) for a specific analog-to-digital converter (ADC) requires attention to impedance matching, charge injection, noise reduction, and output accuracy. ADC manufacturers often recommend a specific amplifier for a given converter, but the combination must be compatible with the target system. Overall performance must be considered as well as the ADC's input structure and its effect on the buffer.

Progress in the development of ADCs-including ever-increasing speed and resolution, switched-capacitor input structures, and single-supply operation-is forcing system designers to evaluate the associated drive amplifier very carefully. The drive amplifier, or buffer, must provide a low source impedance and sufficient output current to drive the ADC inputs, and its high-frequency output impedance must be sufficiently low to avoid excessive conversion error. For many sampling ADCs, the buffer also must amplify extremely low-level signals.

How noise affects performance

Ideally, an op-amp signal source should contribute no error beyond that of the ADC. As a minimum condition for avoiding excess noise in the system, the signal-to-noise ratio (SNR) of the source should be better than the theoretical limit of the ADC. Fortunately, the noise performance of all new-generation op amps is much better than 12 bits, and those with good 16-bit noise performance are not difficult to find. It's important to note, however, that the noise powers of the amplifier and the ADC are cumulative.

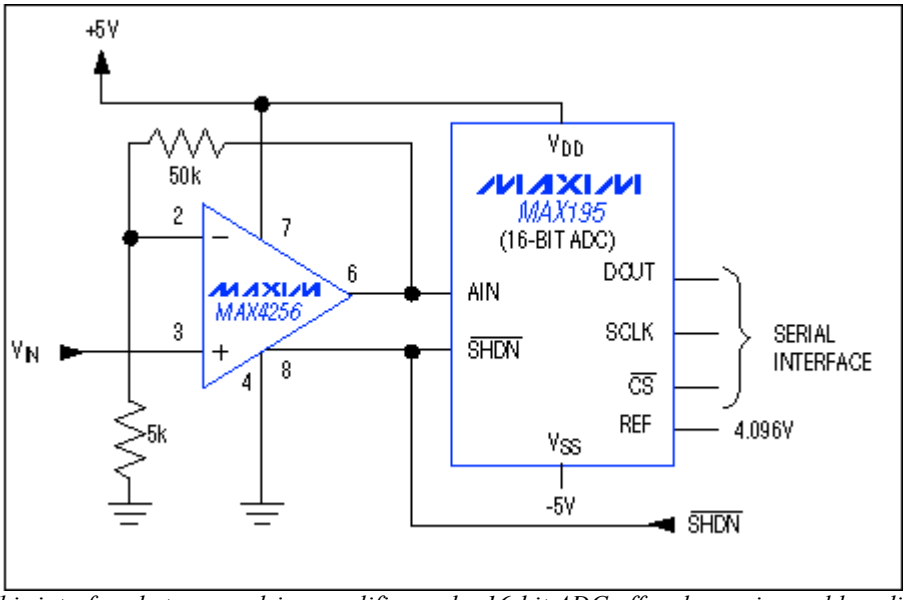

Figure 1. This interface between a drive amplifier and a 16-bit ADC offers low noise and low distortion.

Figure 1 is an excellent example of a low-noise, low-distortion interface between a 16-bit successive-approximation ADC (MAX195) and its input drive amplifier (MAX4256). For this example, calculate the total RMS noise contributed by the buffer using information from the MAX4256 data sheet:
Input voltage-noise density

e_N = 7.9nV/ Hz, at *f*= 30kHz

Input current-noise density

i_N = 0.5 *f*A/ Hz, at *f*= 1kHz.

Because the effective noise bandwidth of a single-pole filter is 1.57 times the -3dB corner frequency, the MAX4256's noise bandwidth is GBW/1.57A_V. In addition to voltage-noise and current-noise sources in the IC, each resistor in the circuit contributes a noise voltage. Thus, the total equivalent input-referred noise is:

$$e_t = \sqrt{e_N^2 + \left[i_N(R1/R2)\right]^2 + (e_r)^2}$$

That is, total noise =

$$\sqrt{\left((\text{volt. noise})^2 + \left(\text{cur. noise} \cdot R_{eq}\right)^2 + (\text{res. noise})^2\right)}$$

To simplify calculation, remember that the noise generated by a 1kΩ resistor in a 1Hz bandwidth is 4nV_{RMS}. That information reduces the formula to:

$$e_r = \left(4nV/\sqrt{Hz}\right)\sqrt{\left(BW \cdot R_{eq}/1k\Omega\right)};$$

where Req(BW) is the equivalent resistance in a specified bandwidth. Assuming a bandwidth of 20kHz for this typical audio-frequency application, and bearing in mind the MAX195 sampling rate (85ksps), the result is e_N = 8.7nV/ Hz. Note that the MAX4256's input current noise of 0.5 *f*A/ Hz is insignificant in comparison. Total output noise referred to the op-amp circuit's bandwidth is:

$$\begin{aligned} E_T &= e_t\sqrt{\left[BW(1/\beta)\right]} \\ &= \left(8.7nV/\sqrt{Hz}\right)\sqrt{20kHz(1.57)(11)} \\ &= 17\mu V_{RMS} \end{aligned}$$

To determine the total noise power for the ADC/op-amp combination, first convert the ADC signal noise and distortion (SINAD) values from decibels to voltage. Then calculate the square root of the sum of the squares and convert the value back to decibels. In this case, we use the MAX195's minimum guaranteed SINAD value of 87dB. Converting to voltage (44.7µV) and combining with E_T = 17µV results in a total noise power of 86.4dB-a degradation of only 0.6LSB in the ADC's SNR. A series of these calculations can demonstrate the effect of a given drive amplifier on the overall performance.

Distortion

Distortion also degrades dynamic performance, but this effect can be minimized by choosing an amplifier whose distortion is much less than the converter's total harmonic distortion (THD). Again, **Figure 2's** circuit is very effective: the MAX195's THD is only -97dB (0.0014%), and the MAX4256's SINAD is an outstanding -115dB. This high performance allows use of the noninverting configuration and a single-supply op amp (MAX4256).

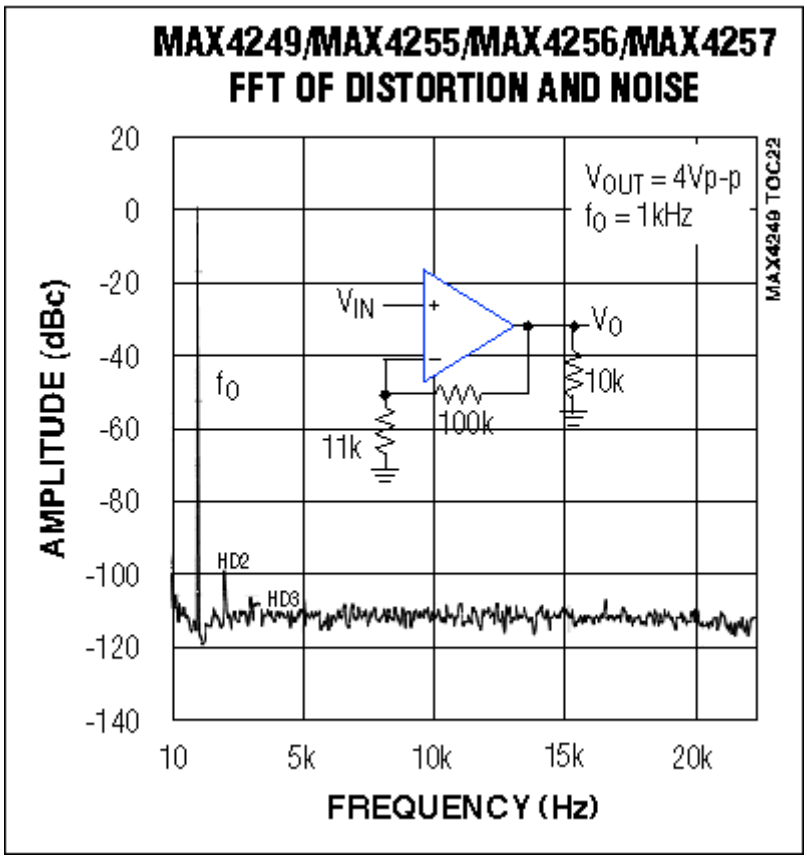

Figure 2. The MAX4256 offers an outstanding spurious-free dynamic range (SFDR) of 115dB.

Another way to evaluate op amps as drive amplifiers is to compare their numerical specifications to the weight (step size) of the ADC's least significant bit (LSB) in volts. For example, the LSB for a 16-bit ADC with a 5.000V unipolar input range is 76µV. To approximate the amplifier's error contribution, compare that number to the amplifier's input offset voltage, drift, and noise, all multiplied by its closed-loop gain. Thus, a closed-loop gain of +11V/V and an offset of 70µV (typical for the MAX4256) produce an error of 770µV, which for a 16-bit application is 10LSBs! If DC accuracy is important, the buffer's offset must either be much less than the ADC's maximum offset (±3LSBs for the MAX195), or it should be trimmed through hardware or software.

The MAX410 family op amps also work well with the ±5V supplies used by the MAX195. The MAX410 has a ±3.5V common-mode input range and a similar output-voltage swing, which allows the converter to operate with reference voltages up to 3.5V. The MAX410's offset voltage (250µV) is approximately 2LSBs. Its drift (1µV/°C), unity-gain bandwidth (28MHz), and low voltage noise (2.4nV/ √Hz) are all compatible with 16-bit performance (**Figure 3**).

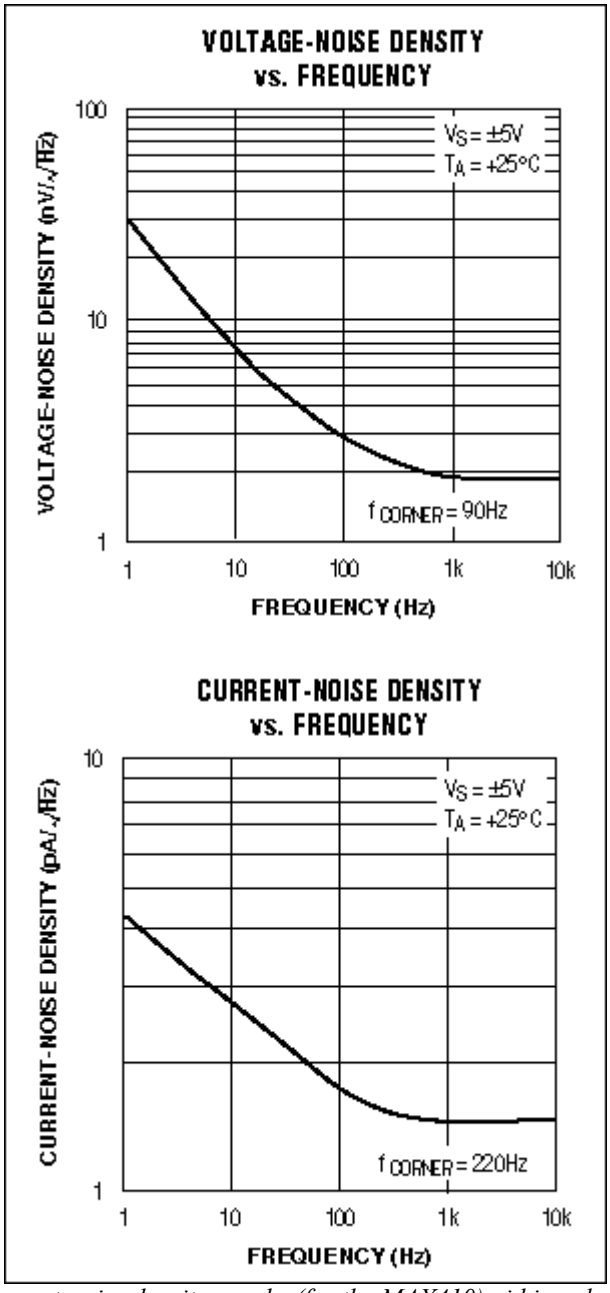

Figure 3. Voltage- and current-noise density graphs (for the MAX410) aid in calculating the accuracy obtainable with a given ADC.

Bandwidth and settling time

To determine speed requirements for the drive amplifier, match its settling time to the ADC's acquisition time. That is, the conversion results will be accurate if the ADC samples the input signal for an interval longer than the amplifier's worst-case settling time. By definition, settling time is the interval between the application of an input voltage step and the point at which the output signal reaches and stays within a given error band centered on the resulting steady-state output level (**Figure 4**).

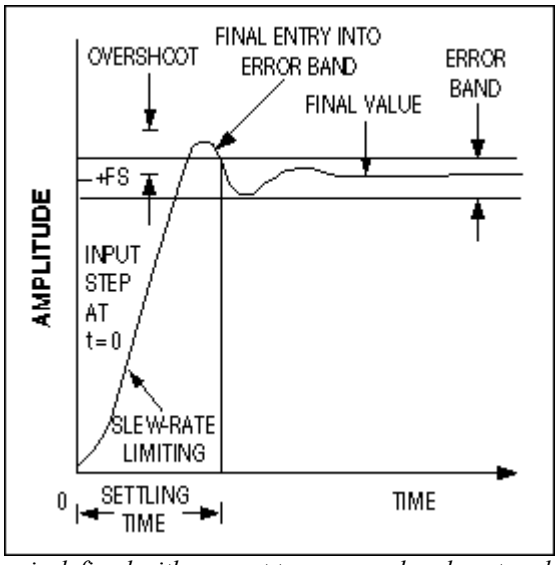

Figure 4. Output settling time is defined with respect to an error band centered on the final settled value.

For large input steps, the amplifier's slew-rate limit restricts the speed with which its output can change. The result, for a given input amplitude and for an amplifier with a given slew rate, is a maximum at the frequency that can be faithfully reproduced:

$$f_{MAX} = SR/2\pi Vp$$

where Vp is the peak output voltage.

A first-order approximation of settling time (t_S) can be made if the following conditions apply:
The input signal does not cause the amplifier output to enter slew-rate limiting

The amplifier's -3dB corner frequency is known

The output amplitude rolls off at 20dB/decade for at least one decade of frequency above f_{-3dB}.

Then,

$$t_S = -1/2\pi f_{-3dB}[\ln(V_O/V_S - 1)] \quad [1]$$

To calculate t_S to within 1/2LSB at N-bit resolution, replace V_O/V_S with the expression $(2^N - 1/2)/2^N$, where N is the number of bits. Equation [1] now becomes:

$$t_S = 0.11(1 + N)/ f_{-3dB} \quad [2]$$

Finding an amplifier that meets the requirements of your application may be difficult. Numerous op amps can operate satisfactorily with 12-bit ADCs, but only a few are suitable for driving 14- and 16-bit ADCs above 500kHz. The choice involves trade-offs among the parameters of noise, distortion, and settling time. Settling time poses a problem because few op-amp manufacturers test this specification at levels equivalent to 16-bit performance (0.001%).

Consider bandwidth and settling time for the drive amplifier in Figure 1. For its typical slew rate of 2.1V/µs, the maximum frequency this buffer can handle with an input amplitude of 2Vp-p is f_{MAX} = SR/2π2Vp = 167kHz. Similarly, for settling time, solve equation [2] for the f_{-3dB} frequency after substituting the 16-bit settling time (1.6µs at 0.001%) for t_S. Though just an approximation, the surprising result is 1.17MHz. Bandwidth requirements for high-resolution settling time can be much higher than expected, and designers often underestimate the bandwidth necessary to sustain gain accuracy. Insufficient

gain over the input-signal bandwidth can easily introduce errors greater than 1LSB. Fortunately, the MAX4256 offers a -3dB corner frequency of 22MHz.

High-speed applications

For demanding video and other high-speed applications, Maxim offers a broad range of video op amps that are also suitable for use as ADC drivers. Among them, the members of a new family of low-noise, low-distortion, 880MHz video op amps make outstanding drive amplifiers (**Table 1** and **Figure 5**):

Table 1. Op amp family for ADC driver applications

PART	MINIMUM STABLE GAIN (V/V)	BANDWIDTH (MHz)	PIN-PACKAGE
MAX4104	1	880	5-pin SOT23, 8-pin SO
MAX4304	2	730	5-pin SOT23, 8-pin SO
MAX4105	5	430	5-pin SOT23, 8-pin SO
MAX4305	10	350	5-pin SOT23, 8-pin SO

- -3dB bandwidth of 880MHz (MAX4104)
- 0.1dB gain flatness to 100MHz (MAX4104/MAX4105)
- 1400V/µs slew rate (MAX4105/MAX4305)
- Spurious-free dynamic range (SFDR) (5MHz, R_L = 100Ω) of -88dBc (MAX4104/MAX4304)
- High output-current drive: ±70mA
- Low input offset voltage: ±1mV

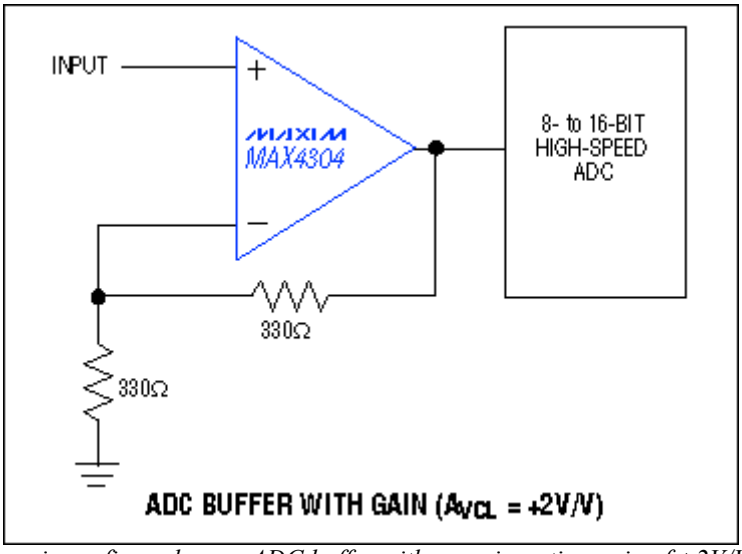

Figure 5. This op amp is configured as an ADC buffer with a noninverting gain of +2V/V.

Also noteworthy as drive amplifiers are the MAX4106/MAX4107 op amps, which combine high speed with an ultra-low noise level of 0.75nV/√Hz. The MAX4106 is compensated for closed-loop gains of +5V/V or greater, the MAX4107 for +10V/V or greater. Low-distortion architecture provides an SFDR of 63dB at 5MHz. Furthermore, these high-speed op amps have a wide output-voltage swing (±3.2V with a ±5V supply) and a substantial current-drive capability of 80mA (**Figure 6**).

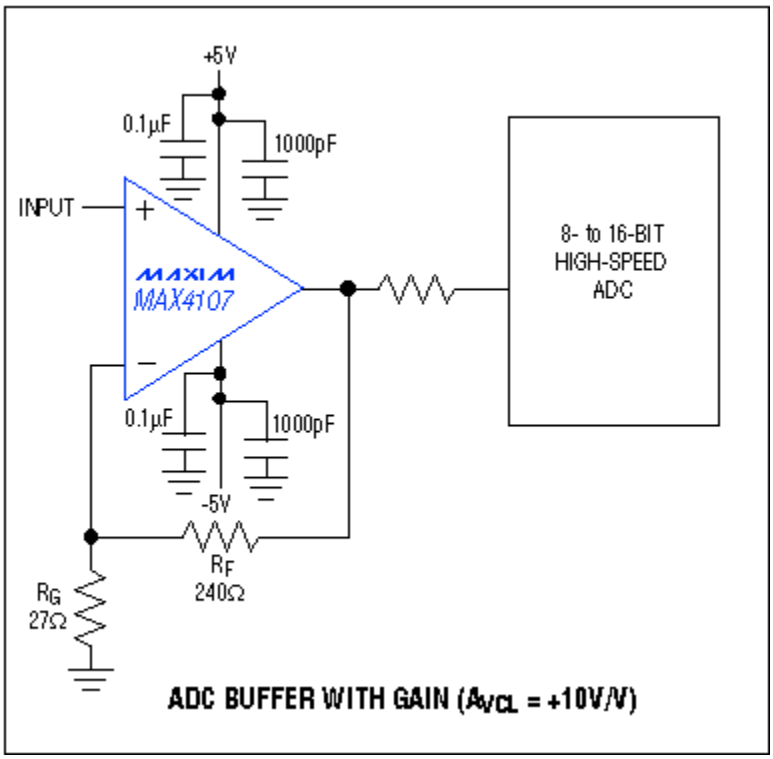

Figure 6. Operating with a noninverting gain of +10V/V, this ADC buffer suits high-frequency applications.

Finally, the MAX4108/MAX4109/MAX4308/MAX4309 op-amp family combines ultra-high speed with ultra-low distortion. At 5MHz, VOUT = 2Vp-p and RL = 100Ω, the MAX4108 SFDR is an unprecedented -93dBc. High speed, high slew rate, low (or ultra-low) noise, and low, stable distortion levels make these op amps well suited for use as buffer amplifiers in high-speed ADC applications (**Figure 7**).

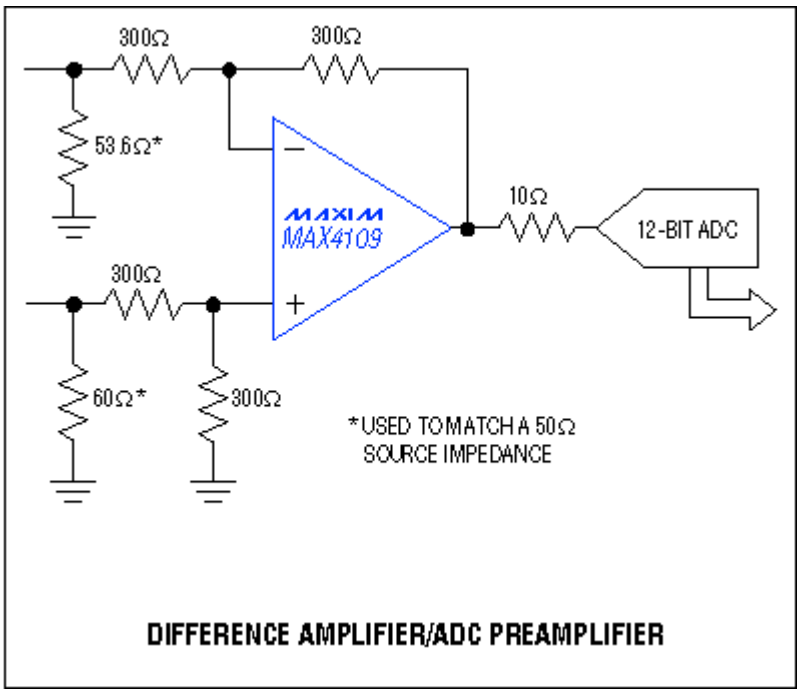

Figure 7. The buffer in this high-speed ADC application operates as a difference amplifier/preamplifier.

Buffer performance also depends on the ADC input structure

In addition to the considerations discussed above, a key concern in selecting a buffer (drive amplifier) is the ADC's input structure. For example, flash converters are among the most difficult to drive because they have a large nonlinear input capacitance. ADCs that have the newer switched-capacitor architectures also require close attention.

The task of driving a switched-capacitor ADC is simplified if you recognize that the ADC draws a small transient of input current at the end of each conversion, when the internal sampling capacitors switch back to the input for acquisition of the next sample. To avoid errors, the buffer circuitry must recover from this transient and settle before the next conversion starts. This can be accomplished using either of two methods.

One method requires driving the ADC with an op amp that settles from a load transient in less than the ADC's acquisition time. (Many new ADCs include such wideband sample/holds on-chip.) Fortunately, most op amps settle from a load transient much more quickly than from an input step, so this requirement is not too difficult to meet with an external buffer. A second method involves adding an RC filter at the input whose capacitor is much larger than the ADC's input capacitance. This larger capacitor eliminates the transient by providing charge for the sampling capacitor (**Figure 8**). To absorb transient glitches, Maxim often recommends using a capacitor of 1000pF or more between the ADC input and ground.

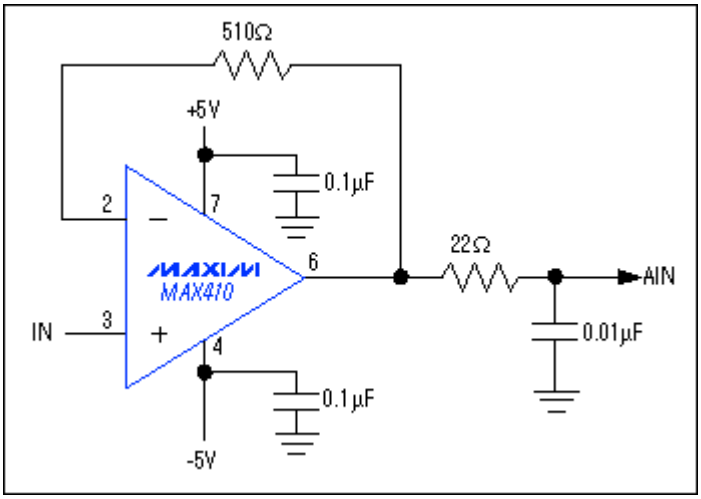

Figure 8. The 22Ω/0.1µF output filter absorbs transients from the ADC and helps stabilize the amplifier.

An RC filter also reduces the possibility of amplifier-stability problems when driving a capacitive load. A small resistor in series with the capacitor helps to prevent ringing and oscillation. At higher capacitive loads, AC performance is controlled by the interaction of the load capacitance and the isolation resistor. Another key concern is to ensure that the amplifier maintains low output impedance over all input frequencies of interest. Op amps with high output impedance cannot respond quickly to changes in the ADC's input capacitance. Nor can they handle the transient currents produced by the ADC. Nonlinearities result when the op amp does not settle in time for the next conversion.

Remember that high loop gain is necessary for low output impedance, according to the equation $R_{OUT} = R_O/(1 + A_{VO}\beta)$, where R_O is the open-loop output impedance and $A_{VO}\beta$ is the loop gain. $A_{VO}\beta$ decreases as you approach the op amp's unity-gain crossover frequency, leading to increased output impedance (**Figure 9**). Higher output impedance makes it difficult for the amplifier to handle current spikes from the ADC.

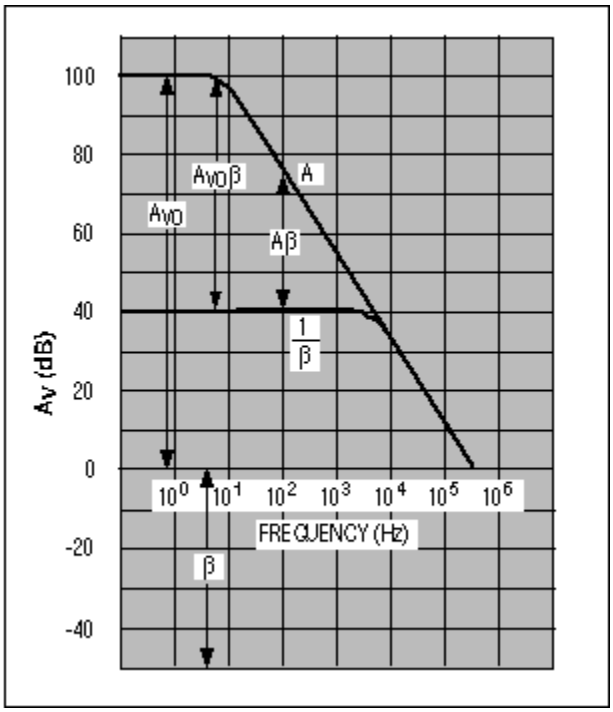

Figure 9. Output impedance generally rises with frequency.

Thus, the low-impedance requirement leads to a requirement for wide bandwidth. Because higher bandwidth op amps have higher loop gain and therefore lower output impedance at higher frequencies, it makes sense to use a 500MHz op amp in front of a 50Msps ADC. The high-bandwidth op amp is more effective than a lower bandwidth amplifier in absorbing current transients produced by the ADC.

Limited loop gain error can affect overall gain accuracy

The Bode diagram of Figure 9 also depicts, for the noninverting circuit, the relationships between open-loop gain (A), the feedback-attenuation factor (β), noise gain (1/β), and loop gain (Aβ, or $A_{VO}\beta$ at DC) as functions of frequency. Figure 9 shows the variation of open-loop gain vs. frequency for a typical operational amplifier. At very low frequencies, the DC open-loop gain (A_{VO}) is near 100dB. Also note that the logarithm of the feedback-attenuation factor is negative because it represents a reduction in the signal amplitude.

Loop gain is depicted in the figure as the sum of the open-loop gain and the feedback attenuation factor (+100dB + (-40dB) = 60dB at very low frequency), or as the difference between the open-loop gain and the noise gain, 1/β [+100dB - (+40dB) = 60dB]. For a given value of β, observe that as frequency increases, the loop gain Aβ decreases. To obtain a greater amount of loop gain at higher frequencies, either increase the open-loop gain of the amplifier or increase the feedback factor β (i.e., decrease the noise gain).

These observations lead to a key equation in feedback systems. Referring to the unity-gain noninverting amplifier,

$$A_{CL} = V_{OUT}/V_{IN} = 1/(1 + 1/A\beta). \quad [3]$$

This equation indicates that the closed-loop gain (A_{CL}) depends on both the open-loop gain and the feedback factor. Both of these quantities are functions of frequency, so loop gain is a function of frequency as well. The amount of loop gain at the operating frequency is the key measure of how closely an amplifier configuration approaches the ideal.

To understand the effect of open-loop gain on overall gain accuracy, consider a practical example based on equation [3]. Assuming an op amp with 40dB open-loop gain at the frequency of interest, the closed-loop gain has an error of 1%. This error drops to 0.1% at 60dB gain, and to 0.01% at 80dB gain. Therefore, 80dB is the minimum allowable open-loop gain that will maintain unity closed-loop gain while properly driving a 12-bit ADC. To accommodate a higher closed-loop gain, modify equation [3] as follows:

$$A_{CL} = V_{OUT}/V_{IN} = (1/(1 + 1/A\beta))(R_F + R_I)/R_I \quad [4]$$

where R_F and R_I are the feedback and input resistors, respectively. Depending on the level of closed-loop gain required, even higher open-loop gain may be needed to maintain the required accuracy.

Output impedance vs. frequency

Low impedance vs. frequency has made video amplifiers such as the MAX4100 very popular as ADC drivers in medical ultrasound applications (**Figure 10**). At the sampling frequency typical for the newest 10-bit ADCs in ultrasound systems (50MHz), the MAX4100 exhibits an output resistance of less than 2Ω. The MAX4100 is a voltage-feedback, high-speed, unity-gain-stable amplifier that delivers a 500MHz unity-gain bandwidth, a 250V/µs slew rate, and a settling time of 35ns (to 0.01%) or 18ns (to 0.1%).

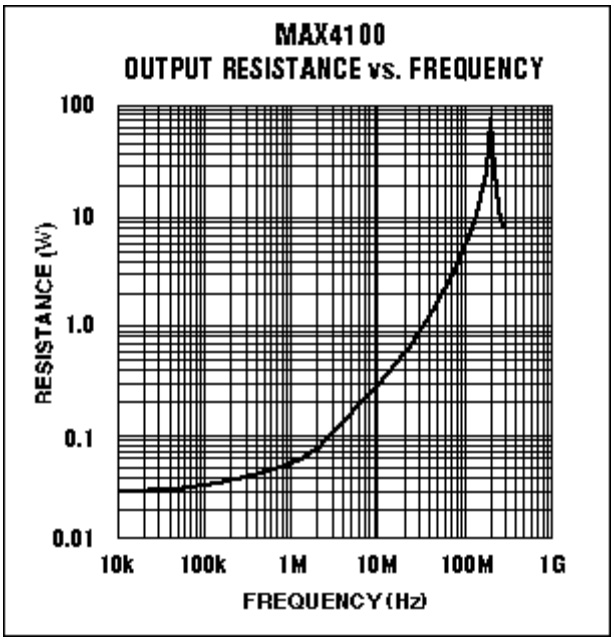

Figure 10. The MAX4100 exhibits less than 0.2Ω output resistance at 50MHz.

Despite the availability of new ADC architectures and other technology improvements, companies like Maxim answer many questions about missing codes and poor linearity. The cause of these problems is generally assumed to be poor performance in the ADC, but it often stems from a poor choice of drive amplifier instead. **Tables 2** and **3** give an overview of the ADC-drive amplifiers, enabling a selection of single-supply (down to +2.7V) vs. dual-supply types, and fastest vs. most-accurate types.

Table 2. ADC drive-amplifier selection, single op amps, single supply (+2.7V to +5.5V)

DEVICE	GAIN STABILITY	GBW (MHz)	VOLTAGE-NOISE DENSITY (nV/√Hz)	CURRENT-NOISE DENSITY (pA/√Hz)	MAX OFFSET (±mV)	OFFSET TEMPCO (µV/°C)	SLEW RATE (V/µs)	SETTLING TIME TO 0.01% (µs)	THD (%)
MAX495	1	0.5	25	0.1	0.500	2.0	0.2	12.0	0.003
MAX4330	1	3	28	0.4	1.500	3.0	1.5	4.0	0.003
MAX4331	1	3	28	0.4	0.600	3.0	1.5	4.0	0.003
MAX4250	1	3	7.9	0.0005	0.750	0.3	6.7	0.3	0.0004
MAX4251	1	3	7.9	0.0005	0.750	0.3	6.7	0.3	0.0004
MAX4122	1	5	22	0.4	1.000	2.0	2.0	2.0	0.003
MAX4123	1	5	22	0.4	0.600	2.0	2.0	2.0	0.003
MAX4322	1	5	22	0.4	2.000	2.0	2.0	1.3	0.003
MAX4323	1	5	22	0.4	2.500	2.0	2.0	1.3	0.003
MAX4165	1	5	26	0.4	1.000	3.0	2.0	2.1	0.003
MAX4166	1	5	26	0.4	1.000	3.0	2.0	2.1	0.003
MAX4130	1	10	22	0.4	1.000	2.0	4.0	2.0	0.003
MAX4131	1	10	22	0.4	0.600	2.0	4.0	2.0	0.003
MAX4255	10	22	7.9	0.0005	0.750	0.3	1.6	2.1	0.0012
MAX4256	10	22	7.9	0.0005	0.750	0.3	1.6	2.1	0.0012
MAX4124	10	25	22	0.4	1.000	2.0	10.0	1.3	0.003
MAX4125	10	25	22	0.4	0.600	2.0	10.0	1.3	0.003
MAX4012	1	200	10	6.0	20.000	8.0	600.0	0.045*	-75dB
MAX4212	1	300	10	6.0	12.000	8.0	600.0	0.045*	-75dB
MAX4213	1	300	10	6.0	9.000	8.0	600.0	0.045*	-75dB

* To 0.1%

Table 3. ADC drive-amplifier selection, single op amps, dual supplies (±5V)

DEVICE	GAIN STABILITY	GBW (MHz)	VOLTAGE-NOISE DENSITY (nV/√Hz)	CURRENT-NOISE DENSITY (pA/√Hz)	MAX OFFSET (±mV)	OFFSET TEMPCO (µV/°C)	SLEW RATE (V/µs)	SETTLING TIME TO 0.01% (µs)	THD (dB)
MAX400	1	0.6	11	0.17	0.015	0.3	0.3	N/A	N/A
MAX410	1	28	2.4	1.2	0.250	1.0	4.5	1.3	-98
MAX4103	2	180	5	1	8.000	5.0	350	0.03	-76
MAX4101	2	200	6	0.8	8.000	15.0	250	0.035	-65
MAX4309	10	200	6	2	8.000	13.0	1200	0.012	-83
MAX4308	5	220	6	2	8.000	13.0	1200	0.012	-83
MAX4109	2	225	6	2	8.000	13.0	1200	0.012	-90
MAX4180	1	240	2	4	7.000	12.0	450	0.02*	-73
MAX4102	1	250	7	1	8.000	5.0	400	0.03	-78
MAX4113	2	270	2.2	13	8.000	10.0	1800	0.035	-62
MAX4181	2	270	2	4	7.000	12.0	450	0.02*	-73
MAX4107	10	300	0.75	2.5	3.000	1.0	500	0.018	-63
MAX4106	5	350	0.75	2.5	3.000	1.0	275	0.018	-63
MAX4305	10	350	2.1	3.1	6.000	2.5	0.025	1400	-67
MAX4108	1	400	6	2	8.000	13.0	1200	0.012	-93
MAX4112	1	400	2.2	13	8.000	10.0	1200	0.035	-68
MAX4105	5	430	2.1	3.1	6.000	2.5	1400	0.025	-74
MAX4100	1	500	8	0.8	8.000	15.0	250	0.035	-70
MAX4224	2	600	2	3	6.000	2.0	1100	0.005*	-68
MAX4304	2	730	2.1	3.1	6.000	2.5	0.025	1000	-88
MAX4104	1	880	2.1	3.1	6.000	2.5	400	0.025	-88
MAX4223	1	1000	2	3	6.000	2.0	1100	0.008*	-65

* To 0.1%

References

1. Maxim Integrated Products, Full-Line Data Catalog on CD-ROM, 1998 Ed., version 2.0.

2. Crystal Semiconductor, Application Note AN06, January 1995.

3. Linear Technology Corp., Application Note 71, July 1997.

4. Burr-Brown Corp., Application Bulletin AB-098, April 1995.

MORE INFORMATION

MAX400:	QuickView	-- Full (PDF) Data Sheet (160k)	-- Free Sample
MAX4012:	QuickView	-- Full (PDF) Data Sheet (448k)	-- Free Sample
MAX410:	QuickView	-- Full (PDF) Data Sheet (1.1M)	-- Free Sample
MAX4100:	QuickView	-- Full (PDF) Data Sheet (160k)	-- Free Sample
MAX4101:	QuickView	-- Full (PDF) Data Sheet (160k)	-- Free Sample
MAX4102:	QuickView	-- Full (PDF) Data Sheet (160k)	-- Free Sample
MAX4103:	QuickView	-- Full (PDF) Data Sheet (160k)	-- Free Sample
MAX4104:	QuickView	-- Full (PDF) Data Sheet (144k)	-- Free Sample
MAX4105:	QuickView	-- Full (PDF) Data Sheet (144k)	-- Free Sample
MAX4106:	QuickView	-- Full (PDF) Data Sheet (144k)	-- Free Sample
MAX4107:	QuickView	-- Full (PDF) Data Sheet (144k)	-- Free Sample
MAX4108:	QuickView	-- Full (PDF) Data Sheet (192k)	-- Free Sample
MAX4109:	QuickView	-- Full (PDF) Data Sheet (192k)	-- Free Sample
MAX4112:	QuickView	-- Full (PDF) Data Sheet (176k)	-- Free Sample
MAX4113:	QuickView	-- Full (PDF) Data Sheet (176k)	-- Free Sample
MAX4122:	QuickView	-- Full (PDF) Data Sheet (296k)	-- Free Sample
MAX4123:	QuickView	-- Full (PDF) Data Sheet (296k)	-- Free Sample
MAX4124:	QuickView	-- Full (PDF) Data Sheet (296k)	-- Free Sample
MAX4125:	QuickView	-- Full (PDF) Data Sheet (296k)	-- Free Sample
MAX4130:	QuickView	-- Full (PDF) Data Sheet (424k)	-- Free Sample
MAX4131:	QuickView	-- Full (PDF) Data Sheet (424k)	-- Free Sample
MAX4165:	QuickView	-- Full (PDF) Data Sheet (240k)	-- Free Sample
MAX4166:	QuickView	-- Full (PDF) Data Sheet (240k)	-- Free Sample
MAX4180:	QuickView	-- Full (PDF) Data Sheet (432k)	-- Free Sample
MAX4181:	QuickView	-- Full (PDF) Data Sheet (432k)	-- Free Sample
MAX4212:	QuickView	-- Full (PDF) Data Sheet (456k)	-- Free Sample
MAX4213:	QuickView	-- Full (PDF) Data Sheet (456k)	-- Free Sample
MAX4223:	QuickView	-- Full (PDF) Data Sheet (256k)	-- Free Sample
MAX4224:	QuickView	-- Full (PDF) Data Sheet (256k)	-- Free Sample
MAX4250:	QuickView	-- Full (PDF) Data Sheet (1.1M)	-- Free Sample
MAX4251:	QuickView	-- Full (PDF) Data Sheet (1.1M)	-- Free Sample
MAX4255:	QuickView	-- Full (PDF) Data Sheet (1.1M)	-- Free Sample
MAX4256:	QuickView	-- Full (PDF) Data Sheet (1.1M)	-- Free Sample
MAX4304:	QuickView	-- Full (PDF) Data Sheet (144k)	-- Free Sample
MAX4305:	QuickView	-- Full (PDF) Data Sheet (144k)	-- Free Sample
MAX4308:	QuickView	-- Full (PDF) Data Sheet (192k)	-- Free Sample
MAX4309:	QuickView	-- Full (PDF) Data Sheet (192k)	-- Free Sample
MAX4322:	QuickView	-- Full (PDF) Data Sheet (512k)	-- Free Sample
MAX4323:	QuickView	-- Full (PDF) Data Sheet (512k)	-- Free Sample
MAX4330:	QuickView	-- Full (PDF) Data Sheet (192k)	-- Free Sample
MAX4331:	QuickView	-- Full (PDF) Data Sheet (192k)	-- Free Sample
MAX495:	QuickView	-- Full (PDF) Data Sheet (240k)	-- Free Sample